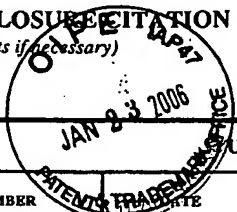


INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)



Docket Number (Optional) 100-24000 (P05764)		Application Number 10/730,658
Applicant(s) James Thomas Doyle		
Filing Date December 8, 2003	Group Art Unit 2816	

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JZ		*6,157,247	12/05/00	Abdesselem et al.	327	540	08/06/97

U.S. PATENT APPLICATION PUBLICATIONS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER Jeffrey Zweizig	DATE CONSIDERED 2/1/06
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INFORMATION DISCLOSURE CITATION

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DEC. 28 2004

PATENT & TRADEMARK OFFICE

Docket Number (Optional)

100-24000 (P05764)

Application Number

10/730,658

Applicant(s)

James Thomas Doyle

Filing Date

December 8, 2003

Group Art Unit

2838

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JZ		Appln. 10/053,858	1/19/02	Maksimovic et al.	—	—	01/19/02
JZ		Appln. 10/106,428	3/26/02	Doyle et al.	—	—	03/26/02
JZ		Appln. 10/272,027	10/15/02	Doyle et al.	—	—	10/15/02

U.S. PATENT APPLICATION PUBLICATIONS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

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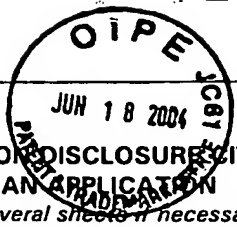
EXAMINER

Jeffrey Zweizig

DATE CONSIDERED

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FORM PTO-1449 INFORMATION DISCLOSURE CITATION IN AN APPLICATION <i>(Use several sheets if necessary)</i>		Docket Number (Optional) 100-24000 (P05764)	Application No. 10/730,658
		Applicant(s) James Thomas Doyle	
		Filing Date December 8, 2003	Group Art Unit 2838
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)			
JZ	Dragan Maksimovic, Bruno Kranzen, Sandeep Dhar and Ravindra Ambatipudi, U.S. Patent Application No. 10/053,226, filed January 19, 2002, entitled "An Adaptive Voltage Scaling Digital Processing Component and Method of Operating the Same".		
JZ	Bruno Kranzen and Dragan Maksimovic, U.S. Patent Application No. 10/053,227, filed January 19, 2002, entitled "Adaptive Voltage Scaling Clock Generator for Use in a Digital Processing Component and Method of Operating the Same".		
see IDS 12/28/04	Dragan Maksimovic and Sandeep Dhar, U.S. Patent Application No. 10/053,828, filed January 19, 2002, entitled "System for Adjusting a Power Supply Level of a Digital Processing Component and Method of Operating the Same".		
JZ	Dragan Maksimovic, Ravindra Ambatipudi, Sandeep Dhar and Bruno Kranzen, U.S. Patent Application No. 10/053,228, filed January 19, 2002, entitled "An Adaptive Voltage Scaling Power Supply for Use in a Digital Processing Component and Method of Operating the Same".		
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JZ	Dragan Maksimovic and James Thomas Doyle, U.S. Patent Application No. 10/166,822, filed June 10, 2002, entitled "Serial Digital Communication Superimposed on a Digital Signal Over a Single Wire".		
JZ	Dragan Maksimovic and Sandeep Dhar, U.S. Patent Application No. 10/236,482, filed September 6, 2002, entitled "Method and System for Providing Self-Calibration for Adaptively Adjusting a Power Supply Voltage in a Digital Processing System".		
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JZ	Wai Cheong Chan and Donald Kevin Cameron, U.S. Patent Application No. 10/324,997, filed December 18, 2002, entitled "System and Method for Signal Delay in an Adaptive Voltage Scaling Slack Detector".		
JZ	Mark F. Rives, U.S. Patent Application No. 10/246,971, filed September 19, 2002, entitled "Power Supply System and Method that Utilizes an Open Loop Power Supply Control".		
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JZ	Robert W. Erickson and Dragan Maksimovic, <u>Fundamentals of Power Electronics</u> , Second Edition, Kluwer Academic Publishers, 2001, pp. 333.		
JZ	Krisztian Flautner, Steven Reinhardt and Trevor Mudge, Automatic Performance Setting for Dynamic Voltage Scaling, Wireless Networks, Volume 8, Issue 5, September 2002, pps. 507-520, and Citation, pps. 1-3, [online]. [retrieved on 2003-02-02]. Retrieved from the Internet: <URL: http://portal.acm.org/citation.cfm?id=582455.582463&coll=portal&dl=ACM&idx=J804&p... >.		
JZ	Krisztian Flautner, Steven Reinhardt and Trevor Mudge, Automatic Performance Setting for Dynamic Voltage Scaling [online]. May 30, 2001, [retrieved on 2003-02-02]. Retrieved from the Internet: <URL: http://www.eecs.umich.edu/~tnm/papers/mobicom01.pdf >. pps. 1-12.		
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JZ	Intel XScale Core, Developer's Manual, December 2000, [online], [retrieved on 2003-02-02]. Retrieved from the Internet: <URL: http://developer.intel.com/design/intelxscale/27347301.pdf >. pps. 1-1 through B-1.		
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INFORMATION DISCLOSURE CITATION <i>(Use several sheets if necessary)</i>				Docket Number (Optional) 100-24000 (P05764)		Application Number 10/730,658	
				Applicant(s) James Thomas Doyle			
				Filing Date December 8, 2003		Group Art Unit 2838	

U.S. PATENT DOCUMENTS							
*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JZ		6,498,512 B2	12/24/02	Simon et al.	326	93	02/27/01
JZ		6,317,008 B1	11/13/01	Gabara	331	117 R	01/26/99
JZ		10/351,061	1/24/03	Chan et al.	—	—	01/24/03
JZ		10/351,056	1/24/03	Chan et al.	—	—	01/24/03
JZ		10/402,091	3/28/03	Doyle	—	—	03/28/03

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*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS								
	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

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JZ		Kaushik Roy, Leakage Tolerant Circuits, Sub-Threshold Logic [online]. No date, [retrieved by inventor approximately 2002-11-01]. Retrieved from the Internet:<URL:http://www.ece.purdue.edu/~visi/seven.pdf>. pps. 1-43.
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EXAMINER Jeffrey Zweig	DATE CONSIDERED 2/1/06
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INFORMATION DISCLOSURE CITATION <i>(Use several sheets if necessary)</i>				Docket Number (Optional) 100-24000 (P05764)		Application Number 10/730,658		
				Applicant(s) James Thomas Doyle				
				Filing Date December 8, 2003		Group Art Unit 2838		
U.S. PATENT DOCUMENTS								
*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
JZ		5,602,882	02/11/97	Co et al.	375	372	01/19/96	
JZ		6,351,165 B1	02/26/02	Gregorian et al.	327	156	08/21/00	
JZ		6,262,611 B1	07/17/01	Takeuchi	327	159	06/23/00	
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*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
FOREIGN PATENT DOCUMENTS								
	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO
OTHER DOCUMENTS <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>								
JZ		John G. Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", 1996 ISCCC8.1 Presentation Slides, 3 sheets, IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pps. 1723-1732.						
EXAMINER				DATE CONSIDERED				
Jeffrey Zweizig				2/1/06				
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